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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/797,945	03/10/2004	Jhon Jhy Liaw	67,200-1253	4848

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EXAMINER	
ARENA, ANDREW OWENS	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 12/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/797,945	LIAW, JHON JHY	
	Examiner	Art Unit	
	Andrew O. Arena	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) *1-17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of group II, claims 18-31 in the reply filed on 03/28/2005 is acknowledged. The traversal is based on applicant's arguments that the structure recited in apparatus claims 18-31 "must be fabricated by a process recited in claim 1," which is not persuasive since applicant merely recites the claim limitations without logically explaining how or why the structure of claim 18 cannot be made by any other process than that recited in claim 1.

Examiner is willing to withdraw the restriction requirement if applicant states for the record that method claims 1-17 and device claims 18-31 are not patentably distinct.

The requirement is still deemed proper and is therefore made FINAL.

Claim Objections

2. Claim 18 is objected to because of the following informalities: the recitation "through the first contact layer" (ln 11-12) appears to be a misprint, and will be interpreted as "through the second contact layer." Appropriate correction is required.

3. Claim 26 is objected to because of the following informalities: the recitation "the gate electrode." There is insufficient antecedent basis for this limitation in the claim. Appropriate correction is required.

4. Claim 30 is objected to because of the following informalities: the recitation "the first and second first and second first and second" appears to be a misprint, and will be interpreted as "the first and second." Appropriate correction is required.

5. Claim 34 is objected to because of the following informalities: the recitation "an overlying an underlying second" appears to be a misprint and will be interpreted as "an overlying or underlying second." Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 31 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. Claim 31 depends from, and refers to the "interconnect lines" of, claim 30. This is unclear because if interconnect lines are not selected in claim 30, claim 31 is rendered indefinite.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 18-25 and 27-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Karasawa et al. (US 6,720,628) – hereinafter Karasawa – in view of Zhou et al. (US 6,358,842) – hereinafter Zhou – and Chen et al. (6,784,096) – hereinafter Chen.

11. Regarding claim 18, Karasawa discloses a contact interconnect structure (Fig 12) comprising:

a semiconductor substrate (inherent in CMOS devices) comprising CMOS devices (Q5; col 4 ln 36-47) including active contact regions (col 6 ln 11-17);

a first dielectric layer (90) comprising a first contact layer overlying the active contact regions comprising a first plurality metal filled openings (82, 80) extending through the first contact layer thickness (col 9 ln 54-56, col 10 ln 16-18) to provide electrical communication to the active contact regions;

a second dielectric layer (92) comprising a second contact layer overlying the first contact layer comprising a second plurality of metal filled openings (84; Fig 13 for plurality) extending through the second contact layer thickness (col 11 ln 42-45) to provide electrical communication to the first contact region;

wherein, each of the first and second plurality of metal filled openings comprise a bottom portion having a maximum width and an aspect ratio (inherent in an opening).

12. Further regarding claim 18, Karasawa differs from the claimed invention in not expressly disclosing the first and second dielectric layers are each a "set of dielectric layers." Zhou discloses an interconnect structure (Fig 13) wherein the metal filled opening dielectric layer is a set of dielectric layers (58, 62, 66). Therefore, it would have

been obvious to a person having ordinary skill in the art at the time the invention was made to provide each of the dielectric layers of Karasawa as a set of dielectric layers, as taught by Zhou; for at least the purpose of enhanced dielectric performance.

13. Further regarding claim 18, Karasawa differs from the claimed invention in not expressly disclosing either a maximum width of "less than about 70 nanometers" or an aspect ratio of "less than about 4.5." Chen discloses an interconnect structure and teaches a via with an opening width of less than about 70 nm and an aspect ratio of less than about 4.5 (col 3 ln 29-33). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to form the metal filled openings of Karasawa with the claimed dimensions, as taught by Chen; for at least the purpose of reducing device size.

14. Regarding claim 19, Karasawa as modified by Chen above discloses said maximum width is less than about 50 nanometers and an aspect ratio of less than about 4.5 (Chen: col 3 ln 29-33).

15. Regarding claim 20, Karasawa discloses (Fig 12) an overlying metallization layer (third conductive layer; col 10 ln 28-37) in electrical communication with the second contact layer (col 10 ln 44 – col 11 ln 29).

16. Regarding claim 21, Karasawa as modified by Zhou above discloses the set of dielectric layers comprises fluorine doped silicon oxide (Zhou: FSG; col 4 ln 24-28).

17. Regarding claim 22, Karasawa as modified by Zhou above discloses (Zhou: Fig 13) the first and second set of dielectric layers comprise lowermost portions (58) of silicon nitride (col 4 ln 13-15).

18. Regarding claim 23, Karasawa as modified by Zhou above discloses (Zhou: Fig 13) the first and second set of dielectric layers comprise overlying portions (62) of fluorine doped silicon oxide (FSG; col 4 ln 24-28).

19. Regarding claim 24, Karasawa discloses the first and second plurality of metal filled openings comprise conductive material Ti (col 9 ln 56-59, col 11 ln 42-47).

20. Regarding claim 25, Karasawa discloses (Fig 12) the active contact regions are gate electrodes (20, 30; col 6 ln 11-17).

21. Regarding claim 27, Karasawa discloses the active contact regions comprise a silicide conductive material (col 6 ln 14-17, col 7 ln 51-51), and does not limit his silicide to any particular type, therefore the disclosure of Karasawa encompasses all well-known silicide types, including NiSi.

22. Regarding claim 28, Karasawa as modified by Zhou above discloses (Zhou: Fig 13) the first and second set of dielectric layers comprise an uppermost portion (66) of a hardmask layer (silicon nitride; col 4 ln 13-15).

23. Regarding claim 29, Karasawa does not limit his metal filled opening shape to any particular type, therefore the disclosure of Karasawa encompasses all well-known metal filled opening shapes, including circular.

24. Regarding claim 30, Karasawa discloses (Fig 12) the first and second plurality of metal filled openings are contact holes (80, 82, 84; col 9 ln 54-56, col 11 ln 42-45).

25. Regarding claim 31, Karasawa discloses (Fig 12) interconnect lines (30, 42) which have a length horizontal to the semiconductor major surface between about 0.15

microns to about 500 microns (30 and 42 are clearly longer than 20 (Fig 13), which itself is larger than 0.15 microns; col 6 ln 51-52).

26. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Karasawa, Zhou, and Chen, as applied to claim 18 above, and further in view of Ono (ref U on 892).

27. Regarding claim 26, Karasawa discloses (Fig 12) the gate electrode (24) comprises a gate structure having a gate length (inherent in gate of transistor). The combined device of Karasawa, Zhou, and Chen differs from the claimed invention only in not expressly disclosing a gate length of "less than about 45 nm." Ono discloses a MOSFET (Fig 2a) with a gate structure having a gate length of less than about 45 nm (caption). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to make the gate length of Karasawa less than about 45 nm, as taught by Ono; for at least the purpose of reducing device size.

28. Claims 32-35 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Karasawa in view of Chen.

29. Regarding claim 32, Karasawa discloses a contact interconnect structure (Fig 12) comprising:

at least a first contact layer (90) comprising a first plurality metal filled openings (82, 80) extending through the first contact layer thickness (col 9 ln 54-56, col 10 ln 16-18) to provide electrical communication to overlying and underlying conductive regions;

wherein, the first plurality of metal filled openings comprise a bottom portion having a maximum width and an aspect ratio (inherent in an opening).

30. Further regarding claim 32, Karasawa differs from the claimed invention only in not expressly disclosing either a maximum width of "less than about 70 nanometers" or an aspect ratio of "less than about 3.3." Chen discloses an interconnect structure and teaches a via with an opening width of less than about 70 nm and an aspect ratio of less than about 3.3 (col 3 ln 29-33). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to form the metal filled openings of Karasawa with the claimed dimensions, as taught by Chen; for at least the purpose of reducing device size.

31. Regarding claim 33, Karasawa as modified by Chen above discloses said maximum width is less than about 50 nanometers and an aspect ratio of less than about 4.5 (Chen: col 3 ln 29-33).

32. Regarding claim 34, Karasawa discloses (Fig 12) the at least a first contact layer comprises an overlying second contact layer (92).

33. Regarding claim 35, Karasawa discloses the underlying conductive regions comprise active conductive regions which are gate electrodes (20, 30; col 6 ln 11-17).

34. Regarding claim 37, Karasawa discloses the overlying conductive regions comprise a metallization layer (col 7 ln 58-67, col 9 ln 30-50).

35. Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Karasawa and Chen, as applied to claim 32 above, and further in view of Ono.

36. Regarding claim 36, Karasawa discloses (Fig 12) the gate electrode (24) comprises a gate structure having a gate length (inherent in gate of transistor). The combined device of Karasawa and Chen differs from the claimed invention only in not expressly disclosing a gate length of "less than about 45 nm." Ono discloses a MOSFET (Fig 2a) with a gate structure having a gate length of less than about 45 nm (caption). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to make the gate length of Karasawa less than about 45 nm, as taught by Ono; for at least the purpose of reducing device size.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew O. Arena whose telephone number is (571) 272-5976. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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